

Course Description

Use the ISE™ software tools to implement a design and gain a firm understanding of the Xilinx FPGA architecture. Learn the best design practices from the pros and understand the subtleties of the Xilinx design flow.

This course covers ISE 10.1 features, such as the Architecture Wizard and the Floorplan Editor. Other topics include design planning, implementation options, and global timing constraints. For more emphasis on improving the overall design performance, take the follow-up course *Designing for Performance*, which builds on the basic principles covered in this course.

Note that one of the prerequisites of *Fundamentals of FPGA Design* is the completion of the basic FPGA architecture modules listed below. Go to www.xilinx.com/education and click the Recorded e-Learning link to view these recorded modules.

Level – Fundamental

Course Duration – 1 day

Course Part Number – FPGA13000-10-ILT

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs

Prerequisites

- Basic FPGA Architecture: Slice and I/O Resources REL*
- Basic FPGA Architecture: Memory and Clocking Resources REL*
- Basic FPGA Architecture: Architecture Wizard and Floorplan Editor REL*
- Working HDL knowledge (VHDL or Verilog)
- Digital design experience

Recommended

- Basic HDL Coding Techniques REL* (parts 1 and 2)
- Spartan-3 FPGA HDL Coding Techniques REL* (parts 1 and 2)
- Virtex-5 FPGA HDL Coding Techniques REL* (parts 1 and 2)

Software Tools

- Xilinx ISE Foundation™ 10.1 software with the ISE Simulator

After completing this comprehensive training, you will have the necessary skills to:

- Use the Xilinx Project Navigator to implement and simulate an FPGA design
- Read reports and determine whether your design goals were met
- Use the Architecture Wizard to create DCM instantiations
- Use the Floorplan Editor and PinAhead to make good pin assignments
- Use the Xilinx Constraints Editor to enter global timing constraints
- Locate and modify the implementation options

Course Outline

- Course Agenda
- Xilinx Tool Flow
- **Lab 1:** Xilinx Tool Flow
- Reading Reports
- **Lab 2:** Architecture Wizard and Floorplan Editor/PACE
- **Lab 3:** Pre-Assigning I/O Pins Using PinAhead
- Global Timing Constraints
- **Lab 4:** Global Timing Constraints

- Implementation Options
- **Lab 5:** Implementation Options
- Synchronous Design Techniques
- Course Summary

Lab Descriptions

- **Lab 1:** Xilinx Tool Flow – Create a new project in the ISE Project Navigator and use the Architecture Wizard and the Floorplan Editor or PACE in the design process. Implement a design by using default software options. The design will be simulated and downloaded to a Spartan®-3E FPGA 1600 demo board.
- **Lab 2:** Architecture Wizard and Floorplan Editor/PACE – Use the Architecture Wizard to customize a DCM and incorporate the DCM into the design. Use the Floorplan Editor to assign pin locations and implement the design.
- **Lab 3:** Pre-Assigning I/O Pins Using PinAhead – This lab introduces the basics of making good I/O pin assignments with PinAhead. Perform Weighted Average Simultaneously Switching Output (WASSO) analysis to avoid ground bounce and use the Design Rule Checker to follow I/O banking rules.
- **Lab 4:** Global Timing Constraints – Enter global timing constraints with the Xilinx Constraints Editor. Review the Post-Map Static Timing Report to verify that the timing constraints are realistic. Use the Post-Place & Route Static Timing Report to determine the delay of the longest constrained path for each timing constraint.
- **Lab 5:** Implementation Options – Adjust process properties and I/O configuration options to improve the design performance.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and training credits.

* Recorded e-Learning