



Virtex-5 FPGA Techniques for High-Performance Data Converters

You can harness the DSP resources of Virtex-5 devices to interface to the analog world.

by Luc Langlois
Global Technical Marketing Manager, DSP
Avnet EM
luc.langlois@avnet.com

The incessant demand for higher bandwidths and resolutions in communication, video, and instrumentation systems has propelled the development of high-performance mixed-signal data converters in recent years. This poses a challenge to system designers seeking to preserve the exceptional signal-to-noise specifications of these devices in the signal processing chain. Xilinx® Virtex™-5 FPGAs provide extensive resources for high-performance mixed-signal systems, supported by efficient development tools spanning all phases of design, from system-level exploration to final implementation.

Key Specifications of Data Converters

A typical mixed-signal processing chain starts at the analog-to-digital converter (ADC). Modern high-performance ADCs provide sampling rates extending into the hundreds of megasamples per second (MSPS) for 12- and 14-bit devices. For example, the Texas Instruments ADS5463

ADC provides 12 bits at 500 MSPS, with 64.5 dB full-scale (dBFS) of signal-to-noise ratio (SNR) to 500 MHz.

Fast sampling rates offer several benefits, including the ability to digitize wide-band signals, reduced complexity of anti-alias filters, and lower noise power spectral density. The result is improved SNR in the system. Your challenge is to implement the high-speed interface between the data converter and FPGA while preserving the SNR throughout the signal processing chain in the FPGA.

Before the digital ADC data is captured in the FPGA, you must take careful precautions to minimize jitter on the data converter sampling clock. Jitter degrades SNR depending on the signal bandwidth of interest. For example, preserving 74 dB of SNR - or approximately 12 effective number of bits (ENOB) - for signal bandwidths extending to 100 MHz requires a maximum 300 fs (femtoseconds) of clock jitter. Modern ADCs provide clever interfaces that simplify distribution of clean low-jitter clocks on the board. Let's examine how key features of Virtex-5 FPGAs are used to implement these interfaces.

High-Performance ADC Interface

High-performance ADC sampling rates often exceed the minimum rate necessary to avoid aliasing, or Nyquist rate, defined as twice the highest frequency component in the analog input signal. The highly over-sampled digital signal entering the FPGA need not maintain a fast sampling rate throughout the signal processing chain; it can be decimated with negligible distortion in the digital domain by a high-quality decimation filter. This offers the benefits of a slower system clock in subsequent processing stages for easier timing closure and lower power consumption.

Xilinx Virtex-5 and Spartan™-3A DSP FPGAs provide the ideal resources to implement high-performance decimation filters for fast ADCs using a technique known as polyphase decomposition. A polyphase decimation filter performs a sampling rate change by allocating the DSP workload among a set of D sub-filters, where D = decimation rate. Each subfilter is only required to sustain a throughput of f_s/D , a fraction of the fast incoming sampling rate f_s from the ADC.

As the decimation filter is often the first stage of digital processing, it calls for

the highest performance resources closest to the FPGA pins. A Virtex-5 FPGA's input/output block contains an IDDR (input double-data-rate register) driven directly from the FPGA input buffer. Several differential signal standards are supported, including LVDS, which can sustain in excess of 1-Gbps data rates while providing excellent board-level noise immunity.

The IDDR is used to de-multiplex the fast incoming digital signal from the ADC into two single-data-rate data streams, each at one-half the ADC sampling rate. This is the ideal format to feed a 2x polyphase decimation filter. Using the Virtex-5 DSP48E, each subfilter can sustain 550 MSPS for a maximum 1.1-GSPS ADC sampling rate. Similarly, the Spartan-3A DSP can sustain 500 MSPS ADC sampling rates.

With the benefits of faster ADC sampling rates come the challenges of smaller data-valid windows to latch the data into the FPGA. Furthermore, the wider the ADC data-word precision, the more daunting the layout task and the higher potential for skew across individual signals of the data bus, resulting in corrupted data. Virtex-5 FPGAs provide a robust solution called IODELAY, a programmable delay element contained in every I/O block. IODELAY can individually time-shift each signal of the data bus to accurately position the data-valid window at the optimal transition of the half-rate data-ready signal (DRY).

Figure 1 illustrates the unique features in Virtex-5 devices that serve to implement a high-performance ADC interface. To minimize sampling jitter, the ADC forwards the source-synchronous DRY signal along with the data, while the clean, low-jitter sampling clock routes directly to the ADC without passing through the FPGA.

High-Performance DAC Interface

For equal data-word precision, digital-to-analog converters (DACs) typically offer higher sampling rates than ADCs, resulting in significant design challenges at the DAC extremity of the signal chain. Several features of the Virtex-5 architecture can help surmount the task. For example, consider

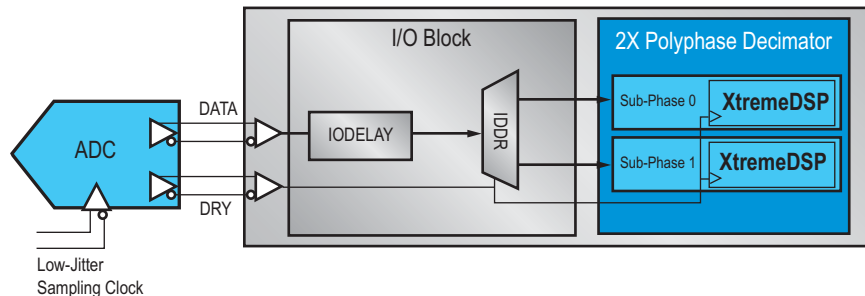


Figure 1 - High-performance ADC interface

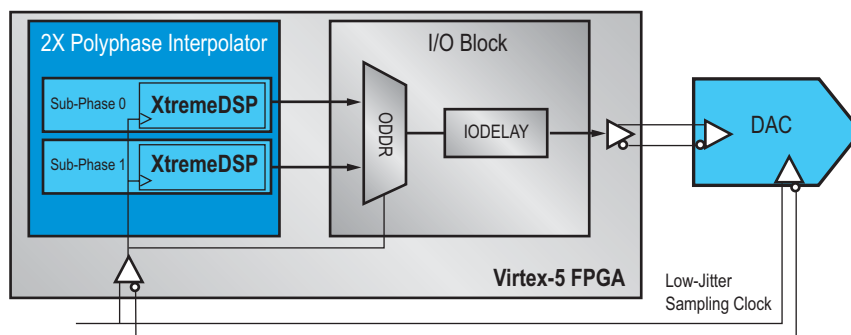


Figure 2 - DAC: polyphase interpolation + ODDR + LVDS

the Virtex-5 interface to a Texas Instruments (TI) DAC5682Z 16-bit dual-DAC with 1-GSPS sampling rate and LVDS inputs.

In a practical system, the 1-GSPS sampling rate need only be deployed at the final output stage to the DAC, while intermediate stages in the FPGA signal processing chain can work at a slower sampling rate commensurate with the signal bandwidth. This allows a slower system clock in the intermediate processing stages, with the benefits of easier timing closure and lower power consumption.

As is the case for the ADC, polyphase filters are efficient DSP structures to realize sampling rate changes at the DAC end of the signal chain. To attain a 1-GSPS output sampling rate to the TI DAC5682Z, a 2x polyphase interpolation filter uses two sub-filters, each with a throughput of 500 MSPS. These rates are within the performance specifications of the Virtex-5 DSP48E slice.

A multiplexer is required to combine the outputs of the sub-filters to attain the fast output rate from the polyphase. For a 1-GSPS output sampling rate, it is advisable

to situate the polyphase interpolator multiplexer as close as possible to the LVDS output buffers driving the DAC5682Z. Virtex-5 FPGAs provide a dedicated resource within the I/O block that is ideally suited to this purpose: the ODDR (output double-data-rate) registers. The ODDR routes directly to fast LVDS differential output buffers able to sustain output rates of 1 GSPS (and beyond) while maintaining signal integrity on the PCB.

Conclusion

In this article, I've presented DSP and interface techniques for mixed-signal systems using Xilinx Virtex-5 FPGAs. You can optimize system performance by preserving the outstanding SNR specifications of modern high-performance data converters using key features of Virtex-5 devices.

The techniques described in this article will be featured in Speedway 2007 DSP sessions, in collaboration with major Avnet data converter suppliers Texas Instruments, Analog Devices, and National Semiconductor. For details, visit <http://em.avnet.com/xilinxspeedway>.